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| EXAMINER | |
|---|---|
| HSIEH, HSIN YI | |

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| 2811 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/574,030 | VAN SCHAIJK ET AL. | |
| | Examiner | Art Unit | |
| | Hsin-Yi (Steven) Hsieh | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12/01/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-8,10,11,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-8, 10-11 and 13-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 8, 10-11, and 13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. **Claim 10** recites the limitation "a spacer" in the third line of the claim. It is unclear whether this limitation is the same as the "spacers" recited in the last line of claim 8, which claim 10 depends on. If the limitations are the same, please use "the spacer" instead of "a spacer". If the limitations are different, please use a different term, e.g. "a first spacer".

4. **Claims 8 and 11** recite the limitation "a floating gate dielectric" in the fourth line of the claim 8 and the 5$^{th}$ line of claim 11. The definition of this term in the claims is inconsistent with what is disclosed in the specification. In the specification, the term "a floating gate dielectric" is a sidewall dielectric next to the formed floating gate and may be formed at the same time as the forming of the access gate dielectric (spec page 4, second and third paragraphs) and as shown as the oxide 102 in Fig. 10. In claims 8 and 11, the limitation "a floating gate dielectric" has "a floating gate" on top of it, which indicates the term "a floating gate dielectric" refers to the tunnel dielectric layer 51. The inconsistency of the definitions of this term renders claims 8 and 11 indefinite. The Examiner also notice that Applicant uses the same term "the floating gate dielectric" referring to either the oxide 102 or the tunnel dielectric layer 51 in claims 10 and 13.

5. **Claims 10 and 13** recite "a wet-etched portion of the floating gate dielectric" in the third lines of claim 10 and the fourth line of claim 13. Firstly, claims 10 and 13 are device claims and this limitation is a process limitation which should not have a patentable weight. The same product can be made with the portion of the floating gate dielectric dry-etched. Secondly, the portion of the floating gate dielectric (assuming it is the tunnel dielectric layer 51) under the wet-etch is removed (spec page 9 lines 20-22). Thus the wet-etched portion of the floating gate dielectric does not exist when the access gate is formed. Using a non-existent structure to construct the structural relationship in claim 10 renders the claim indefinite.

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 1, 3, 5, 7, 8, 10, 11, and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,991,204 A) in view of Sharma et al. (US 5,488,579 A), and

further in view of Quirk et al. ("Semiconductor Manufacturing Technology", 2001, Prentice Hall, pages 456 and 459-460) as can be understood since claims 8, 10-11, and 13 have been rejected under 35 U.S.C. 112.

9. Chang teaches, regarding to **claim 1**, a method of manufacturing on a substrate (semiconductor substrate 100; Fig. 1a, col. 3 line 58) a 2-transistor memory cell (Flash EEPROM cell; Abstract) comprising a storage transistor (the transistor formed under 101) having a memory gate stack (the gate stack under 101) and a selecting transistor (the transistor under 107), there being a tunnel dielectric layer (floating gate oxide layer 104; Fig. 1a, col. 4 lines 2-3) between the substrate (100) and the memory gate stack (the gate stack under 101), the method comprising: forming the memory gate stack (the gate stack under 101) by providing a first conductive layer (floating gate poly 103 in Fig. 6a before the etching) on the tunnel dielectric layer (104; see Fig. 1a) and a second conductive layer (second poly; col. 8 lines 55-58) with a deposited interlayer dielectric layer (layer 102 of ONO; Fig. 1a, col. 3 lines 64-65) between the first and second conductive layers (103 and 101; see Fig. 1a), the deposited interlayer dielectric layer (102) including oxide (oxide/nitride/oxide; col. 3 lines 64-65) and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps (the interlayer dielectric layer 102 is between two polysilicon layers and is susceptible to undesirable growth if two polysilicon layers exposed to oxygen during subsequent oxidation steps), etching the second conductive layer (second poly) thus forming a control gate (101; Fig. 6a, col. 8 lines 55-58), forming spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) against the control gate (101) in the direction of a channel (active channel region 113; Fig. 1a, col. 3 line 62; the direction of channel is the direction from the source to drain) to be formed under the tunnel

dielectric layer (104; see Fig. 1a), and thereafter using the spacers (106) as a hard mask (col. 8 lines 62-65) to etch the first conductive layer (floating gate poly 103 in Fig. 6a before the etching) thus forming the floating gate (floating gate poly 103 in Fig. 6b after the etching), removing a portion of the tunnel dielectric (104) laterally adjacent to the floating gate (103) and exposing a portion of the substrate (100) where the tunnel dielectric (104) has been removed (see Fig. 6b, col. 9 lines 1-2); and forming an access gate dielectric oxide (erase gate oxide 112; Fig. 6c, col. 9 lines 3-4) on the exposed portion of the substrate (100; see Fig. 6c), using the spacers (106) to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer (102; the spacer 106 covers the interlayer dielectric layer 102 that oxygen has to diffuse across the spacer before reaching the interlayer dielectric layer, which means the diffusion of oxygen to 102 is mitigated by the extra diffusing process across the spacer), regarding to **claim 8**, a 2-transistor memory cell (Flash EEPROM cell; Abstract) comprising, a storage transistor (the transistor formed under 101) and a selecting transistor (the transistor under 107), the storage transistor (the transistor formed under 101) comprising a floating gate dielectric (floating gate oxide layer 104; Fig. 1a, col. 4 lines 2-3) on a substrate (semiconductor substrate 100; Fig. 1a, col. 3 line 58), a floating gate (floating gate poly 103 in Fig. 6b, col. 8 lines 62-65) on the floating gate dielectric (104; see Fig. 6b), a deposited interlayer dielectric layer (layer 102 of ONO; Fig. 1a, col. 3 lines 64-65) on the floating gate (103; see Fig. 1a and 6b), a control gate (101; Fig. 6a, col. 8 lines 55-58) on the interlayer dielectric layer (102; see Fig 1a) and being smaller than the floating gate (control gate is shorted than the floating gate; see Fig. 1a), and spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) next to the control gate (101; see Fig. 1a), and that mitigates oxygen diffusion to the interlayer dielectric layer (102; the spacer 106 covers the interlayer dielectric

layer 102 that oxygen has to diffuse across the spacer before reaching the interlayer dielectric layer, which means the diffusion of oxygen to 102 is mitigated by the extra diffusing process across the spacer), and regarding to **claim 11**, an electronic device (Flash EEPROM arrays; col. 3 lines 54-55) comprising a 2-transistor memory cell (Flash EEPROM cell; Abstract), the 2-transistor memory cell including, a storage transistor (the transistor formed under 101) and a selecting transistor (the transistor under 107), the storage transistor (101) comprising a floating gate dielectric (floating gate oxide layer 104; Fig. 1a, col. 4 lines 2-3) on a substrate (semiconductor substrate 100; Fig. 1a, col. 3 line 58), a floating gate (floating gate poly 103 in Fig. 6b, col. 8 lines 62-65) on the floating gate dielectric (104; see Fig. 6b), a deposited interlayer dielectric layer (layer 102 of ONO; Fig. 1a, col. 3 lines 64-65) on the floating gate (103; see Fig. 1a and 6b), a control gate (101; Fig. 6a, col. 8 lines 55-58), on the interlayer dielectric layer (102; see Fig 1a) and being smaller than the floating gate (control gate is shorted than the floating gate; see Fig. 1a), spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) next to the control gate (101; see Fig. 1a), and that mitigates oxygen diffusion to the interlayer dielectric layer (102; the spacer 106 covers the interlayer dielectric layer 102 that oxygen has to diffuse across the spacer before reaching the interlayer dielectric layer, which means the diffusion of oxygen to 102 is mitigated by the extra diffusing process across the spacer).

Chang does not teach, regarding to **claim 1**, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, the etching of the first conductive layer being an anisotropic dry etch that is selective to the tunnel dielectric, thereby using the tunnel dielectric to protect portions of the substrate laterally adjacent

to the floating gate; regarding to **claim 3**, the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or meal oxide, regarding to **claim 8**, the spacers are made from a dielectric material having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers, and regarding to **claim 11**, the spacers are made from a dielectric material having an oxygen diffusion through the dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through oxide spacers.

In the same field of nonvolatile memory, Sharma et al. teach , regarding to **claim 1**, the spacers (nitride sidewall spacer 37; Fig. 2, col. 4 line 52) being formed from a dielectric material (silicon nitride) having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide), regarding to **claim 3**, the dielectric material (silicon nitride; col. 4 line 52) having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or meal oxide (silicon nitride), regarding to **claim 8**, the spacers (nitride sidewall spacer 37; Fig. 2, col. 4 line 52) are made from a dielectric material (silicon nitride) having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide), and regarding to **claim 11**, the spacers (nitride sidewall spacer 37; Fig. 2, col. 4 line 52) are made from a dielectric material (silicon nitride) having an oxygen diffusion through the

dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide).

Sharma et al. also teach that the nitride spacer smoothes the topography created by the polysilicon gate and eliminates any sharp corners or edges of polysilicon gate from protruding into overlying layers (col. 4 lines 55-58).

In the same field of semiconductor manufacturing, Quirk et al. teach, regarding to **claim 1**, the etching of the first conductive layer (poly gate etch; Fig. 16.29, page 460, fourth paragraph) being an anisotropic dry etch (page 459, bottom paragraph and page 460, 4th paragraph) that is selective to the tunnel dielectric (i.e. gate oxide; page 460, 4th paragraph), thereby using the tunnel dielectric (gate oxide) to protect portions of the substrate laterally adjacent to the floating gate (avoiding any microtrenching of the gate oxide around the periphery of the polysilicon; page 460, the bottom paragraph).

Quirk et al. also teach that dry etch can provides high selectivity and low device damage (page 456, the bottom two paragraphs)

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang, Sharma et al. and Quirk et al. using the nitride spacers as taught by Sharma et al. and the dry etch as taught by Quirk et al., because the nitride spacer smoothes the topography created by the polysilicon gate and eliminates any sharp corners or edges of polysilicon gate from protruding into overlying layers as taught by Sharma et al and dry etch can provides high selectivity and low device damage as taught by Quirk et al.

10. Regarding **claim 5**, Chang also teaches a method according to claim 1, further including forming a floating gate dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) next to the formed floating gate (103) while forming the access gate dielectric (erased gate oxide 112; Fig. 6c, col. 9 lines 3-6).

11. Regarding **claim 7**, Chang also teaches a method according to claim 1 wherein, forming an access gate (107) includes forming the access gate while the spacer (106) at the access gate (107) side is still present (see Fig. 6c).

12. Regarding **claim 10**, Chang also teaches a memory cell according to claim 8, the selecting transistor (the transistor under 107) comprising an access gate (erase gate 107; Fig. 6c, col. 4 line 7) on an access gate dielectric (erase gate oxide 112; Fig. 6c, col. 9 lines 3-4) on the substrate (100; see Fig. 6c) immediately adjacent to a wet-etched portion of the floating gate dielectric (i.e. the region of access gate dielectric 112), a spacer (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) being present between the control gate (101) and the access gate (107) and a floating gate sidewall dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) that is contiguous with the access gate dielectric (112) and present between the floating gate (103) and the access gate (107), wherein the spacer (106) is thicker than the floating gate dielectric (109; see Fig. 1a).

13. Regarding **claim 13**, Chang also teaches the selecting transistor (the transistor under 107) includes, an access gate (erase gate 107; Fig. 6c, col. 4 line 7) on an access gate dielectric (erase gate oxide 112; Fig. 6c, col. 9 lines 3-4) on the substrate (100; see Fig. 6c) immediately adjacent to a wet-etched portion of the floating gate dielectric (i.e. the region of access gate dielectric 112), a spacer (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) being present between the

control gate (101), and a floating gate sidewall dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) that is contiguous with the access gate dielectric (112) and present between the floating gate (103) and the access gate (107), wherein the spacer (106) is thicker than the floating gate dielectric (109; see Fig. 1a).

14. **Claims 4 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, Sharma and Quirk et al. as applied to claim 1 above, and further in view of Hong et al. (US 5,614,746 A) as can be understood since claims 8, 10-11, and 13 have been rejected under 35 U.S.C. 112.

Chang teaches, regarding to **claim 4**, before forming the memory gate stack, applying the tunnel dielectric layer (104) on the substrate (100; this is shown in Fig. 6a), and after formation of the memory gate stack (see Fig. 6b), removing the tunnel dielectric layer (104) by a selective etching technique (stripping, col. 9 lines 1-2) at least at a location where the selecting transistor is to be formed (all the exposed area including the selecting transistor region; col. 9 lines 1-2), and regarding **claim 14**, removing a portion of the tunnel dielectric (104; see Fig. 6b, col. 9 lines 1-9) includes removing a portion of the tunnel dielectric laterally adjacent to the floating gate (103) and expose a portion of the substrate surface (100) (see Fig. 6b, col. 9 lines 1-9), and further including forming an access gate (erase gate 107; Fig. 6c, col. 4 line 7) of the selecting transistor (the transistor under 107) on the access gate dielectric (erase gate oxide 112; Fig. 6c, col. 9 lines 1-9).

Chang, Sharma and Quirk et al. do not teach, regarding to **claim 4**, the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate, and regarding to **claim 14**, wet etching the tunnel dielectric to remove a portion of the tunnel

dielectric and expose a portion of the substrate surface where the tunnel dielectric has been wet etched, leaving the exposed surface of the substrate intact.

In the same field of nonvolatile memory, Hong et al. teach, regarding to **claim 4**, the selective etching technique (wet etching; Fig. 3E, col. 6 lines 58-61) preferentially etching the tunnel dielectric layer (tunnel oxide layer 22; Fig. 3E, col. 6 lines 58-61) compared to the substrate (top surface of P-substrate 21; Fig. 3E, col. 6 lines 65-66), and regarding to **claim 14**, wet etching the tunnel dielectric (tunnel oxide layer 22; Fig. 3E, col. 6 lines 58-61) to remove a portion (exposed portion) of the tunnel dielectric (22) and expose a portion of the substrate surface (top surface of P-substrate 21; Fig. 3E, col. 6 lines 65-66) where the tunnel dielectric (22) has been wet etched (see Fig. 3E), leaving the exposed surface of the substrate intact (see Fig. 3E).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang, Sharma, Quirk et al. and Hong et al. to use the wet etch to remove the tunnel oxide because Chang, Sharma and Quirk et al. is silent of how to remove the tunnel oxide and Hong et al. provide a method of wet etch to remove the tunnel oxide.

15. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, Sharma and Quirk et al. as applied to claim 1 above, and further in view of Chen (US 6,091,104 A) as can be understood since claims 8, 10-11, and 13 have been rejected under 35 U.S.C. 112.

Regarding **claim 6**, Chang teaches a method according to claim 1, furthermore comprising removing part of the interlayer dielectric layer (102) before forming the spacers (this

can be shown in Fig. 6a and Fig. 6b, where 102 is left only under the control gate 101 and is enclosed by the spacer 106).

Chang, Sharma and Quirk et al. do not teach removing part of the interlayer dielectric layer after forming the control gate.

In the same field of nonvolatile memory, Chen teaches removing part of the interlayer dielectric layer after forming the control gate (col. 4 lines 64-67). Chen also teaches that the control gate is used as mask that only one lithographical mask is needed to form the gate stack (col. 4 lines 44-67).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang, Sharma, Quirk et al. and Chen and remove the interlayer dielectric layer after forming the control gate as taught by Chen, because only one lithographical mask is needed to form the gate stack as taught by Chen.

### *Response to Arguments*

16. Applicant's arguments with respect to claims 1, 3-5, 7-8, 10-11, and 13 have been considered but are moot in view of the new ground(s) of rejection.

17. Applicant's amendments, filed 12/01/2008, do not respond to the rejection to claim 10 under 35 U.S.C. 112. The rejection to claim 10 under 35 U.S.C. 112 still stands because the referring of the limitation "a spacer" to two different elements is indefinite.

***Conclusion***

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
3/23/2009